Distributed Buck Converter Realization Based on a Transmission Line

Klaus Röbenack
Institute of Control Theory
TU Dresden
Dresden, Germany
klaus.roebenack@tu-dresden.de
ORCID 0000-0002-3347-0864

Richard Herrmann
Germany
richard.herrmann@mailbox.org

***Abstract*—The buck converter is a widely used switched converter to adapt a higher DC voltage to a lower DC voltage. In the conventional design, the converter has two reactive elements, an inductor and a capacitor. Replacing these dynamical elements by a transmission line results in a distributed buck converter. Modeling the transmission line by the telegrapher's equations yields a model with completely new properties. We investigate the behavior of this system and present a practical circuit realization.**

***Index Terms*—buck converter, transmission line, partial differential equations, distributed systems, circuit simulation**

I. Introduction

In electrical engineering, DC-DC converters are used to adapt different levels of voltages, currents, or impedances from a source to a load [1], [2]. Voltage and power levels range from very low for consumer electronics such mobile phones to very high in power grid applications [3].

Today's converters use switching techniques, which leads to a significantly higher efficiency compared to linear voltage controllers. Common DC-DC converters are the buck, boost, and buck-boost converter as well as the Čuk and SEPIC converter. In addition to DC-DC converters there are also converters to adapt between DC, AC, and three-phase electric power [1], [2], [4]. In addition to circuit-related issues, feedback control is playing an increasingly important role for converter circuits [5]–[8].

Converters are an area of active research in power electronics. Usually, the aim is to increase efficiency, reduce voltage fluctuations, and minimize costs. In recent years, numerous new converter topologies have been proposed and investigated [9]–[11].

A *buck converter* or *step-down converter* is a DC-DC converter which steps down the voltage from the supply to the load. It is a class of switched-mode power supply. The converter consists of two reactive elements and an electronic switch built on the basis of semiconductor components. The reactive elements, one inductor and one capacitor, store the electrical energy during the switching process.

Power supply and load may not only require different voltages, but may also be located in different positions. In these cases, the electrical energy is delivered through a transmission line. Taking the transmission line into account leads to more complicated models [12], [13]. In the recent years, new converter topologies have been suggested, where the reactive elements are replaced by a transmission line [14]–[18]. The steady-state behavior of this spatially distributed buck converter was investigated for resistive load in [18] and inductive load in [19], respectively. In the recent publication [20], a control scheme for this converter type was suggested.

This paper extends the conference paper [21] presented at ICSTCC 2022. In [21], we considered the analysis, simulation and implementation of a distributed buck converter. Additionally, a circuit realization using a MOSFET was suggested. In this paper, we investigate the relation between the characteristic impedance and the load resistance as well as the impact of the switching time and the duty ration on the voltage ripples. Furthermore, we tested another circuit realization based on a bipolar junction transistor.

This paper is structured as follows. In Section II we model the conventional buck converter and the new topology with a transmission line. In Section III we investigate the behavior of the converters by means of circuit simulations. The practical circuit realization of the distributed buck converter is presented in Section IV. Finally, we draw some conclusions in Section V.

II. Buck Converter Topologies and Models

A. Conventional Buck Converter

The circuit diagram of a conventional buck converter is shown in Fig. 1. The converter has two semiconductor elements, a transistor and a freewheeling diode. Alternatively, the converter could also be realized with two transistors [22]. In Fig. 1 we used an NPN bipolar junction transistor (BJT). A buck converter can also be implemented with a MOSFET, an insulated-gate bipolar transistor (IGBT) or a gate turn-off thyristor (GTO). In addition, the converter have two passive elements, an inductor and a capacitor. We consider the buck converter with ohmic load.

In the buck converter, the transistor is operated as a switch. Together with the freewheeling diode, the semiconductors can be modeled as a single pole changeover (SPCO). The resulting network model is shown in Fig. 2. The inductor and the capacitor are modeled as ideal elements, i.e., without dissipation. In particular, the inductor was considered without

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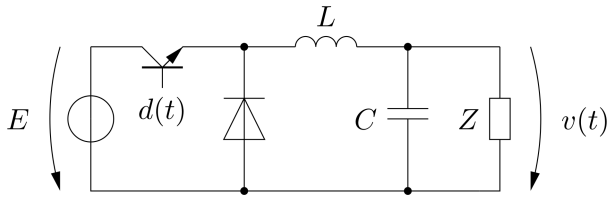

Fig. 1. Circuit diagram of the conventional buck converter

resistance and the capacitor without leakage current. The inductor has the inductance L, the capacitor the conductance C and the load the resistance Z. The converters constant input voltage is denoted by E, the output voltage by $v(t)$, and the current flowing through the inductor by $i(t)$. Furthermore, we assume $E, L, C, Z > 0$.

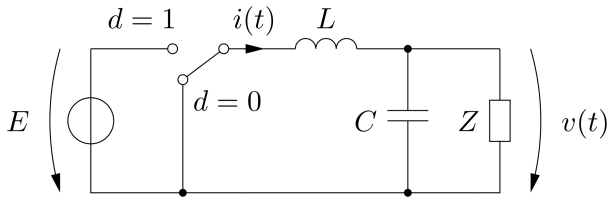

Fig. 2. Network model of the lossless conventional buck converter

Based on the network model shown in Fig. 2 we derive the circuits equations

$$L\tfrac{\mathrm{d}\,i(t)}{\mathrm{d}\,t} + v(t) = E\,d(t) \quad (1a)$$
$$C\tfrac{\mathrm{d}\,v(t)}{\mathrm{d}\,t} + \tfrac{1}{Z}v(t) = i(t) \quad (1b)$$

of the lossless buck converter. These equations form a system of first order *ordinary differential equations (ODEs)*. The circuit equations (1) can be transformed from time to frequency domain using Laplace transform

$$X(s) = \mathcal{L}\{x(t)\} = \int_0^\infty x(t)\ \mathrm{e}^{-st}\,\mathrm{d}\,t$$

for a signal $x \in \{v, i, d\}$, where we use capital letters for the transformed signals. This results in

$$\underbrace{\begin{pmatrix} sL & 1 \\ -1 & sC + \frac{1}{Z} \end{pmatrix}}_{\boldsymbol{M}(s)} \begin{pmatrix} I(s) \\ V(s) \end{pmatrix} = \begin{pmatrix} E \\ 0 \end{pmatrix} D(s).$$

The characteristic polynomial of this system

$$\det \boldsymbol{M}(s) = LC\,s^2 + \tfrac{L}{Z}\,s + 1 \quad (2)$$

is a second order polynomial. Although we consider the lossless converter model, the characteristic polynomial corresponds to a damped harmonic oscillator due to the load. Under the above assumptions, the characteristic polynomial is always a Hurwitz polynomial.The polynomial (2) has real roots if and only if

$$Z \le \frac{1}{2}\sqrt{\frac{L}{C}}. \quad (3)$$

Otherwise, the roots are a complex conjugate pair in the complex open left half plane.

Up to now, the signal d represents the position of the switch with two possible values $d \in \{0, 1\}$. In practical applications the converter is usually operated under *pulse width modulation (PWM)*. Roughly speaking. PWM is a method for getting analog signal with digital means. Let t_{on} and t_{off} denote the time intervals, where the switch in the position 1 and 0, respectively, over one switching period with duration time $T = t_{\text{on}} + t_{\text{off}}$, see Fig. 3. Then, the signal d is considered to be value-continuous representing the ratio between the time t_{on} and the time T of the switching period:

$$d = \frac{t_{\text{on}}}{T}. \quad (4)$$

The signal d defined by (4) is called *duty ratio* or *duty cycle* with the range $d \in [0, 1]$ of admissible values. Nowadays, PWM is implemented with microcontrollers using timers. Several microcontroller families have PWM registers for direct control over the duty cycle and frequency.

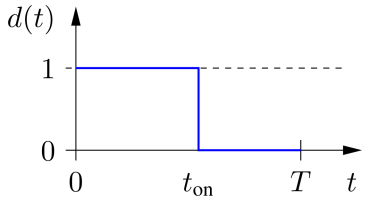

Fig. 3. Signal d over one period of the PWM switching time T

B. Buck Converter with Transmission Line

The inductor and the capacitor in the network model shown in Fig. 2 can be seen as an approximation of a lossless transmission line. Replacing these passive components of the buck converter by a transmission line results in the schematics shown in Fig. 4. In practise we could only expect a low loss transmission line. We assume that the transmission line has length $l > 0$. The dynamic properties of the transmission line are described by inductance L' and conductance C' per length, respectively.

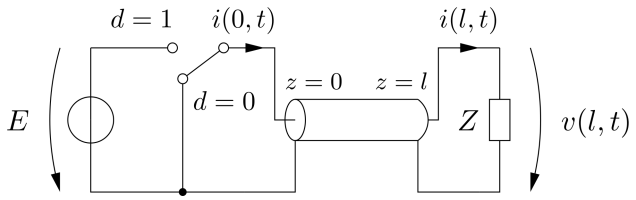

Fig. 4. Network model of a buck converter with transmission line

The lossless transmission line can be modeled by a special case of *telegrapher's equations* [23], [24]:

$$\frac{\partial}{\partial z}v(z,t) + L'\frac{\partial}{\partial t}i(z,t) = 0, \quad (5a)$$
$$\frac{\partial}{\partial z}i(z,t) + C'\frac{\partial}{\partial t}v(z,t) = 0. \quad (5b)$$

In the transmission line, the current and the voltage are distributed signals depending not only on time t but also on the position z, which is in the range between $z = 0$ and $z = l$. Equations (5) form a system of first order *partial differential equations (PDEs)*. These equations can be combined such that one obtains two *wave equations*

$$\frac{\partial^2}{\partial t^2} v(z,t) - c^2 \frac{\partial^2}{\partial z^2} v(z,t) = 0, \tag{6a}$$

$$\frac{\partial^2}{\partial t^2} i(z,t) - c^2 \frac{\partial^2}{\partial z^2} i(z,t) = 0, \tag{6b}$$

where

$$c = \frac{1}{\sqrt{L'C'}} \tag{7}$$

denotes the *propagation speed* of waves travelling through the lossless transmission line.

The electrical connection of the transmission line can be described by the Dirichlet boundary conditions

$$u(0,t) = E\, d(t), \tag{8a}$$

$$u(l,t) - Z\, i(l,t) = 0. \tag{8b}$$

Equations (5) and (8) state a boundary value problem (BVP) being a special case of a Cauchy problem.

Similar as above we want to transfer the model (5) into the frequency domain via Laplace transform of a signal $x \in \{v, i\}$ w.r.t. time t:

$$X(z,s) = \mathcal{L}\{x(z,t)\} = \int_0^\infty x(z,t)\, \mathrm{e}^{-st}\, \mathrm{d}\, t.$$

The time derivative is given by

$$\mathcal{L}\left\{\frac{\partial}{\partial t} x(z,t)\right\} = sX(z,s) - x(z,0).$$

Assuming the initial values to be zero, i.e., $x(\cdot, 0) = 0$, we obtain

$$\frac{\partial}{\partial z} U(z,s) + sL'\, I(z,s) = 0,$$

$$\frac{\partial}{\partial z} I(z,s) + sC'\, U(z,s) = 0.$$

This set of linear ordinary differential equations in the variable z can be solved using the exponential approach. The system matrix

$$\boldsymbol{M} = \begin{pmatrix} sL' & \lambda \\ \lambda & sC' \end{pmatrix} \tag{9}$$

yields the characteristic equation

$$\det(\boldsymbol{M}) = s^2 L'C' - \lambda^2 = 0.$$

The roots of this equation are the eigenvalues

$$\lambda_{1,2} = \pm s\sqrt{L'C'} = \pm s\tau \tag{10}$$

with the *propagation delay* $\tau = \sqrt{L'C'}$, which is the inverse of the propagation speed (7). Another important parameter of the transmission line is the *characteristic impedance*

$$Z_0 = \sqrt{\frac{L'}{C'}}. \tag{11}$$

Let $\boldsymbol{V}_1(s)$ and $\boldsymbol{V}_2(s)$ be the associated eigenvectors of the system matrix (9), e.g.

$$\boldsymbol{V}_{1,2}(s) = \begin{pmatrix} \mp\sqrt{C} \\ \sqrt{L} \end{pmatrix}.$$

In the frequency domain, the solution of the partial differential equation (5) has the following form

$$\boldsymbol{X}(z,s) = c_1(s)\, \boldsymbol{V}_1(s)\, \mathrm{e}^{+s\tau z} + c_2(s)\, \boldsymbol{V}_2(s)\, \mathrm{e}^{-s\tau z} \tag{12}$$

with $\boldsymbol{X}(z,s) = (I(z,s), U(z,s))^T$. The scaling factors $c_1(s)$ and $c_2(s)$ of the eigenvectors have to be chosen such that the boundary conditions (8) are fulfilled.

The exponential functions occurring in the solution (12) can be interpreted as a frequency-dependent spatial delay in the wave propagation. The evaluation of the solution term at the right boundary $z = l$ yields

$$\mathrm{e}^{\pm\gamma(j\omega)l} = \mathrm{e}^{\pm j\omega\tau l}$$

with the *phase delay* $T_D = \tau l$.

III. Transient Simulation

A. Simulation Setup

For the practical circuit realization of the new converter we want to use $6\,\mathrm{m}$ coaxial cable RG 58 CU [25] as a transmission line. The RG 58 is the standard coaxial cable for many applications. The cable has capacitance per length $C' = 100\,\mathrm{pF/m}$ and inductance per length $L' = 241\,\mathrm{nH/m}$. These values correspond to a characteristic impedance $Z_0 \approx 50\,\Omega$, the propagation delay $\tau \approx 5\,\mathrm{ns/m}$ and the phase delay $T_D = \tau l \approx 30\,\mathrm{ns}$.

We also want to compare the behavior of the new converter with the conventional buck converter. For the reactive lumped elements we used the overall capacitance $C = l \cdot C' = 600\,\mathrm{pF}$ and the inductance $L = l \cdot L' = 1446\,\mathrm{nH}$.

To compare our findings with the results published in [21] we used the input supply voltage $E = 12\,\mathrm{V}$. The simulations were carried out with the open source circuit simulator Ngspice (version 37) [26], which is based on Berkeley's Spice3f5. For the visualization we used GNU Octave [27].

B. Step Responses for Different Load Impedances

We consider the step responses of the converter models with $d = 1$ for $t \geq 0$. All initial values we set to zero. We considered different load impedances: $Z \in \{10\,\Omega, 25\,\Omega, 50\,\Omega, 75\,\Omega\}$. The simulation results are shown in Fig. 5.

First, we consider the step responses to the conventional converter model plotted with green lines. Fig. 5 shows the current $i(t)$ through the inductor (left column) and the output voltage $v(t)$ at the load (right column). Since the characteristic polynomial (2) is a Hurwitz polynomial for physically meaningful parameters, the solution converges to the operating point

$$\lim_{t\to\infty} i(t) = \frac{E}{Z}, \tag{13}$$

$$\lim_{t\to\infty} u(t) = E. \tag{14}$$

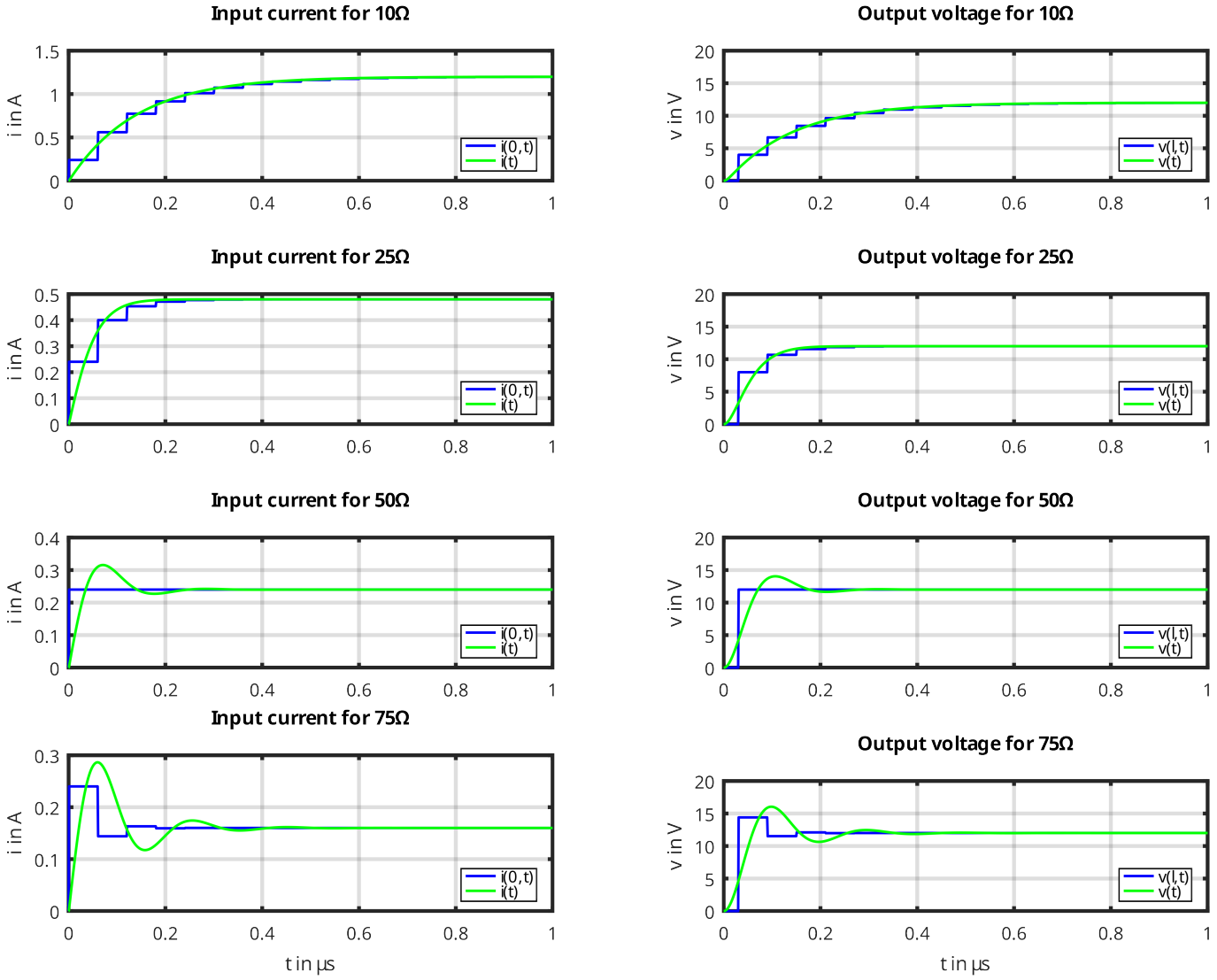

Fig. 5. Transient simulation with currents and voltages for different load impedances, current $i(t)$ and voltage $v(t)$ of the conventional converter, current $i(0,t)$ on the left boundary and voltage $v(l,t)$ on the right boundary of the transmission line of the new converter type

The characteristic polynomial (2) has real roots if condition (3) is fulfilled, i.e.,

$$Z \leq \frac{1}{2}\sqrt{\frac{L}{C}} = \frac{1}{2}\sqrt{\frac{L'}{C'}} = \frac{1}{2}\,Z_0.$$

For $Z = 10\,\Omega$, the inequality becomes strict such that we have the overdamped case. For $Z = 25\,\Omega$, the inequality becomes an equation corresponding to the critically damped case. For $Z > 25\,\Omega$, the system is underdamped resulting in overshooting and oscillations.

Second, we consider the step responses to the new converter model plotted with blue lines. Fig. 5 shows the input current $i(0,t)$ into the transmission line (left column) and the output voltage $v(l,t)$ at the load (right column). The step response leads to piecewise constant functions, due to the constant input signal and the reflected waves.

Applying the initial as well as the final value theorems of the Laplace transform to the solution (12) in the frequency domain we can compute the following limits in the time domain:

$$\lim_{t\to 0} i(0,t) = \frac{E}{Z_0}, \tag{15}$$

$$\lim_{t\to \infty} i(0,t) = \frac{E}{Z}. \tag{16}$$

For $Z < 50\,\Omega$, the input current starts at the lower value (15) and converges to the state-state value (16). For $Z = 50\,\Omega$, we have a perfect matching between the characteristic impedance Z_0 and the load impedance Z. For $Z > 50\,\Omega$, the input current starts at the higher value (15) before converges to the state-state value (16), which results in overshooting and decaying oscillations.

C. Pulse Width Modulation with Different Switching Times and Duty Ratios

The transient simulation results of the converter with transmission line under pulse width modulated excitation are shown in Fig. 6. For the switching time $T = k\,T_D$ we used different multiples $k \in \{2, 3, 4, 5\}$ of the phase delay T_D together with the duty ratios $d = 0.25$ and $d = 0.75$, respectively. The simulation was carried out over a time interval of $1\,\mu s$.

We want to investigate the impact of the PWM switching time to the voltage ripple on the right boundary of the transmission line due to travelling waves. In particular, we want to minimize these voltage ripples. In [20], [21], [28], for the duty ratio $d = 0.5$ the optimal value $T = 4T_D$ was found. This seems not to be the case for the duty ratios $d = 0.25$ and $d = 0.75$ as visualized in Fig. 6, where the voltage ripples for $T = 3T_D$ and $T = 5T_D$ appear to be less as in case of $T = 4T_D$.

In the circuit simulation we have very short voltage peaks in the full range from $0\,V$ to $12\,V$ and beyond. In practice, these peaks would probably not occur due to parasitic elements resulting in a low-pass filter. For a more realistic evaluation we want to suppress these voltage spikes of the circuit simulation using a low-pass filter. The phase delay T_D corresponds to the frequency $f_D = 1/T_D \approx 33.95\,MHz$. We used a second order Butterworth filter with the tenfold cut-off frequency $f_c = 10 f_D \approx 339.5\,MHz$. The filtered voltage values in the last half of the simulated time interval, i.e., $0.5\,\mu s \le t \le 1\,\mu s$, were used to compute mean and extremal values. In Fig. 6, the minimum and maximum values of the filtered voltages are marked with red lines, the mean values with green lines.

Next, we investigate the impact of the switching time and the duty ration on the voltage ripples. Fig. 7 shows the peak-to-peak voltages of the filtered signals depending on the multiples k of the switching time $T = kT_D$ ranging from $k = 1$ to $k = 9$ for different duty ratios from $d = 0.1$ to $d = 0.9$. The largest voltage ripples occur with $k = 1$ and $k = 2$. In case of $k = 4$, we have very small voltage ripples for $d = 0.5$, but large ones otherwise. A good choice with comparatively small over all considered duty ratios seems to be $k = 5.4$, which corresponds to a switching frequency $f = 1/T = 1/(5.4T_D) \approx 6.287\,MHz$, which is also a reduction compared to previous publications.

IV. Circuit Realization

The practical realization can be done in different ways. A simple variant is presented and analyzed concerning its properties in the following.

A. Requirements

The previous discussions have shown that a switching period in the order of the duration of four times of the phase delay of the distributed parametric line is suitable. The experimental setup has a $6\,m$ long coaxial cable of type RG 58 C/U, which has a phase delay of $T_D \approx 30\,ns$. As suggested in [21], [28], we use the quadruple of the phase delay for the switching time, allowing two reciprocating waves. This results in a PWM switching frequency of $f = 1/4T_D \approx 8.3\,MHz$. In addition, the control is to take place on the high potential side.

B. Implementation with NPN Bipolar Transistor

Since the input is to be switched on the high potential side, a common collector circuit is used. It is characterized by the fact that the collector of the transistor is at a fixed potential. In this case, this is the supply voltage E. A small base-emitter current drives a large collector-emitter current. The circuit features a high current gain and a voltage gain of approximately one. Figure 8 shows the schematic of the circuit.

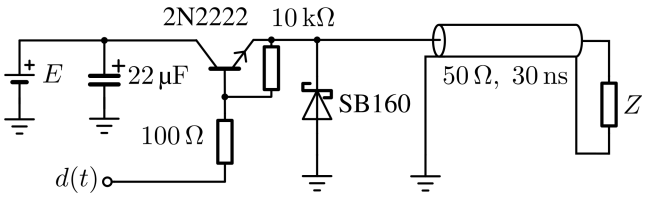

Fig. 8. Circuit diagram with NPN bipolar transistor for generating a rectangular input signal and coaxial cable with load resistor at the end

In addition to the common collector circuit, a Schottky freewheeling diode, the distributed step-down converter in the form of a coaxial cable, and a load resistor are shown. A laboratory power supply provides the voltage E. A function generator supplies the switching signal $d(t)$. Figure 9 shows the hardware on which the practical implementation was investigated.

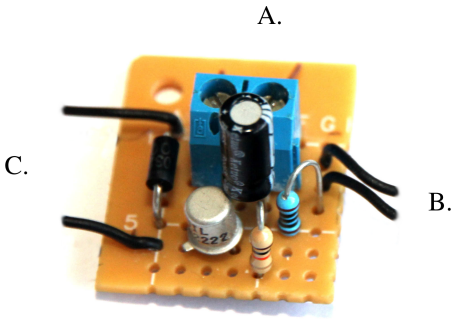

Fig. 9. Circuit for generating a rectangular signal with NPN bipolar transistor (A. Supply B. Signal C. Output)

C. Analysis

The circuit can be simulated with the open source circuit simulator Qucs [29]. The results from the simulation and practical measurement of the experimental circuit are plotted in Figure 10. The two curves match well. This shows that on the one hand the model is comparatively accurate and on the other that the circuit works as desired.

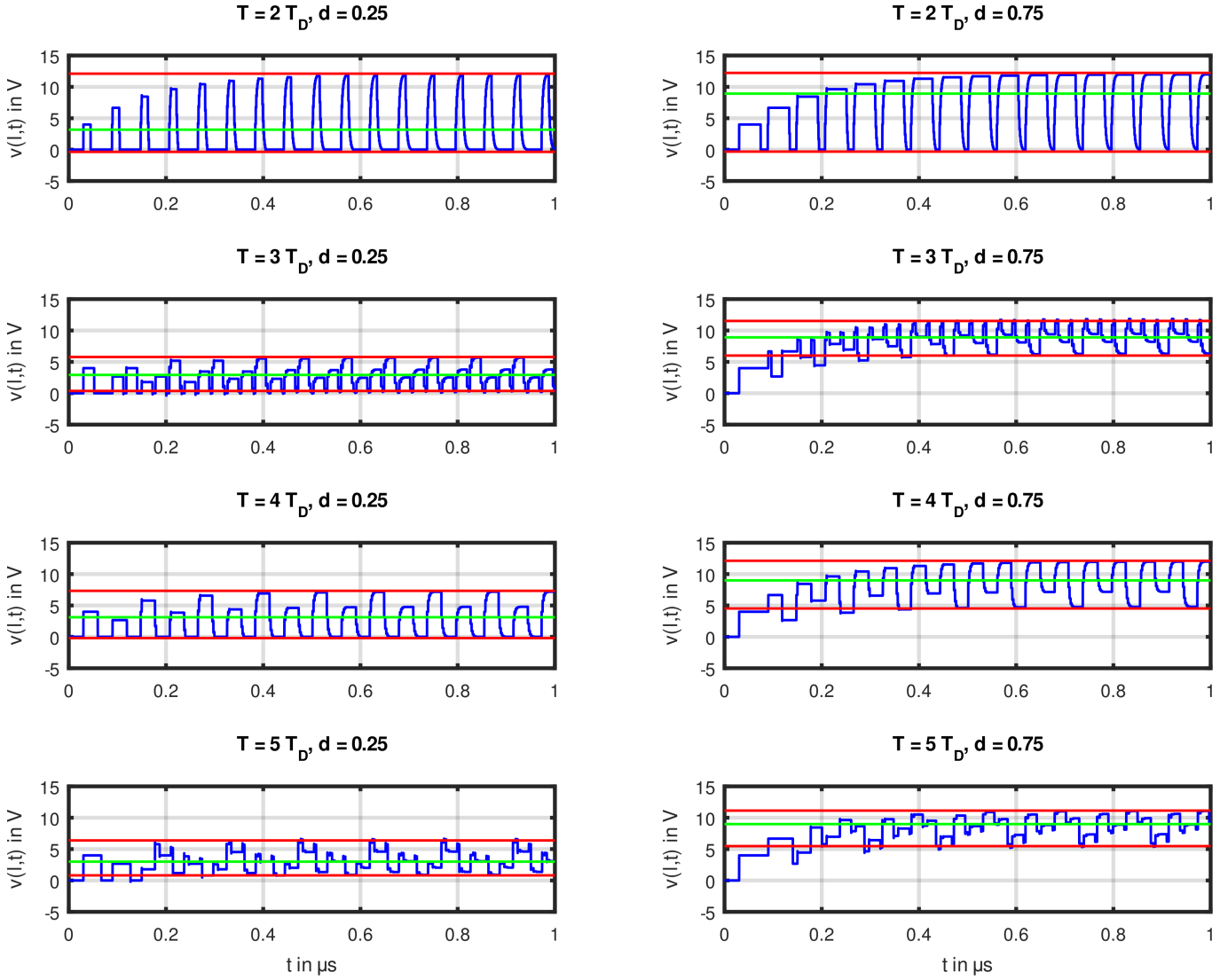

Fig. 6. Transient simulation of the converter with transmission line under pulse width modulated excitation, different switching times T as integer multiples of the phase delay T_D and duty ratios $d \in \{0.25, 0.75\}$

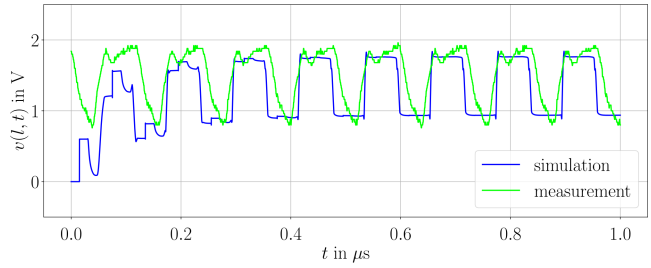

Fig. 10. Voltage over the load simulated and measured

The parameters used on the laboratory power supply unit and the signal generator are summarized in Table I.

TABLE I
PARAMETERS SET FOR THE RESULTS FROM FIGURE 10

Parameter	Value	Parameter	Value
Supply voltage E	4 V	Rise time	8.4 ns
Signal voltage $d_{\max}$	5 V	Falling time	8.4 ns
Period duration	120 ns	Load Z	10 Ω
Power-on time	42 ns		

Across the transistor, the input voltage is reduced by the collector-emitter voltage U_{CE}. This voltage, multiplied by the current, results in power dissipation. In addition, there are further losses due to switching. According to the datasheet [30], the selected transistor 2N2222 is designed for a collector current of 800 mA and power dissipation of 1.2 W. In the operated circuit, the transistor heats up significantly.

The principle function of a step-down conversion could be demonstrated, but the circuit has yet to be further investigated

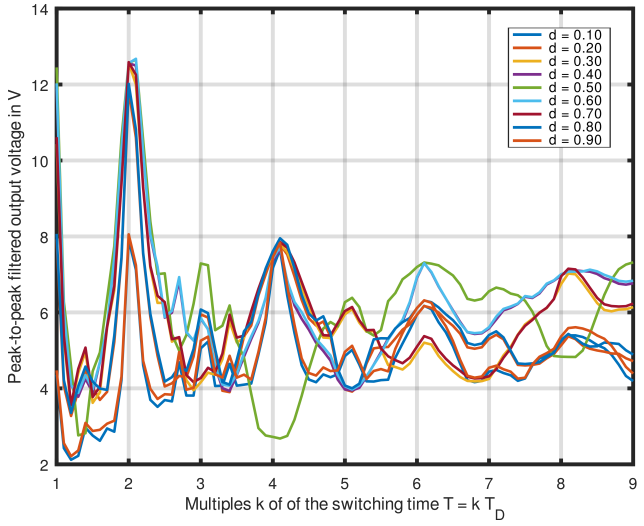

Fig. 7. Peak-to-peak voltage ripples of the filtered output voltage for different multiples k of the switching time $T = kT_D$ for different duty ratios d

due to severe limitations. An alternative can be realized with p-channel MOSFETs with low resistance between drain and source in the switched-on state and high gain bandwidth [21], [28].

V. Conclusions

In this paper, we investigated a modified buck converter with a transmission line both from an analytical as well as a numerical point of view. The transient analysis was carried out by circuit simulation. The simulation results were confirmed by a practical realization of the converter using electronic standard components.

The discussed implementation can be seen as proof of concept augmenting the implementation suggested in [21]. Further research should be devoted to better implementation of the power electronics, the reduction of the switching frequency and closed-loop control.

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